

1       1. A method of developing a response compactor  
2 comprising:  
3               adding at least two columns to a compactor matrix  
4 for each circuit output that can produce an unknown logic  
5 value at the same time.

1       2. The method of claim 1 including adding at least  
2 two columns to a compactor matrix for each scan chain that  
3 can produce an unknown logic value at the same time.

1       3. The method of claim 2 including obtaining the  
2 maximum number of scan chains that can produce unknown  
3 logic values at the same time.

1       4. The method of claim 2 wherein adding at least one  
2 column to the matrix for each such scan chains that can  
3 produce an unknown logic value includes adding two columns  
4 to the matrix for each such scan chain.

1       5. The method of claim 2 including reducing the  
2 compactor matrix using maximum compatibility class problem.

1       6. The method of claim 5 including eliminating from  
2 the matrix one of at least two matching columns.

1        7. The method of claim 1 wherein adding at least two  
2 columns to a compactor matrix includes adding at least two  
3 columns to the compactor matrix for every combination of  
4 the number of unknown logic values plus one.

1        8. The method of claim 7 including adding values to  
2 the matrix rows such that for a first row the first column  
3 has a value one and the succeeding columns have the value  
4 zero and a second row has the column value zero followed by  
5 the column value one and a third row has the column values  
6 zero, zero, followed by the column value one.

1        9. A response compactor formed by the process  
2 including the steps of:  
3                obtaining a number of circuit outputs that can  
4 produce unknown logic values at the same time; and  
5                adding at least two columns to a compactor matrix  
6 for each such circuit output that can produce unknown logic  
7 values at the same time.

1        10. The compactor of claim 9 formed by a process  
2 wherein obtaining a number of circuit outputs that can  
3 produce unknown logic values at the same time includes  
4 determining the maximum number of circuit outputs that can  
5 produce errors at the same time.

1        11. The compactor of claim 9 wherein the compactor is  
2 formed by a process wherein adding at least one column to  
3 the matrix for each circuit output that can produce unknown  
4 logic values at the same time includes adding two columns  
5 to the matrix for each such circuit output.

1        12. The compactor of claim 9 formed by a process  
2 including reducing the compactor matrix using maximum  
3 compatibility class problem.

1        13. The compactor of claim 12 wherein said compactor  
2 is formed of a process including eliminating from the  
3 matrix one of at least two matching columns.

1        14. The compactor of claim 9 formed by a process  
2 wherein adding at least two columns to a compactor matrix  
3 includes adding at least two columns to the compactor  
4 matrix for every combination of the number of circuit  
5 outputs that can produce unknown logic values at the same  
6 time plus one.

1        15. The compactor of claim 14 formed by a process  
2 including adding values to the matrix rows such that for a  
3 first row the first column has a value one and the  
4 succeeding columns have the value zero and a second row has  
5 the column value zero followed by the column value one and

6 a third row has the column value zero, zero followed by the  
7 column value one.

1 16. A response compactor comprising:  
2 a plurality of exclusive OR gates arranged to  
3 handle any number of scan chains with unknown logic values.

1 17. The compactor of claim 14 that can handle any  
2 number of errors in the same scan cycle.

1 18. The compactor of claim 14 including the minimum  
2 number of scan outputs.

1 19. An article comprising a medium storing  
2 instructions that, if executed, enable a processor-based  
3 system to:  
4 add at least two columns to a compactor matrix  
5 for each scan chain that can produce an unknown logic value  
6 at the same time.

1 20. The article of claim 19 further storing  
2 instructions that, if executed, enable a processor-based  
3 system to obtain the maximum number of scan chains that can  
4 produce unknown logic values at the same time.

1        21. The article of claim 19 further storing  
2 instructions that, if executed, enable a processor-based  
3 system to add two columns to the matrix for each such  
4 unknown logic value.

1        22. The article of claim 19 further storing  
2 instructions that, if executed, enable the compactor matrix  
3 to be reduced using maximum compatibility class problem.

1        23. The article of claim 19 further storing  
2 instructions that, if executed, enable a processor-based  
3 system to eliminate from the matrix one of at least two  
4 matching columns.

1        24. The article of claim 19 further storing  
2 instructions that, if executed, enable a processor-based  
3 system to add at least two columns to the compactor matrix  
4 for every combination of the number of unknown logic values  
5 plus one.

1           25. The article of claim 23 further storing  
2 instructions that, if executed, enable a processor-based  
3 system to add values to the matrix rows such that for a  
4 first row the first column has a value one and the  
5 succeeding columns have the value zero and a second row has  
6 a column value zero followed by the column value one and  
7 the third row has the column value zero, zero, followed by  
8 the column value one.